

Mixed Signal Infrastructure Circuits for Energy Autonomous Ultra Low Power Systems on Chip

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Abstract

Ultra-Low Power (ULP) Systems on Chip (SoC) such as wireless sensor nodes are being used for an ever increasing number of applications. They can be used for applications – measuring and reporting almost everything from the flow of crude oil in a remote pipeline to the degree of corrosion in a steel bridge to EKG, EEG and EMG signals of a home health patient. Owing to their remote locations and small form factor, these nodes need to consume extremely low power. They should operate from harvested energy as changing their batteries regularly is not a viable option. Energy autonomy is central to the wide spread deployment of these sensor nodes. However, a significant percentage of energy is lost in harvesting, supplying regulated output voltages, and in the “idle mode” of the state of the art sensor nodes. Therefore, energy efficiency is the most important challenge facing the design of these sensor nodes.

The design of processor, radio, memory, etc. for a sensor node has received much attention. However, a sensor node also needs clock sources and power supplies to be able to operate. These circuits constitute the “infrastructure” around which a digital system can be created. In wireless sensors, these circuits perform energy harvesting, provide regulated output voltages and clock sources for the SoC. The design of these infrastructure circuits can impact the energy efficiency and hence the life time of the SoC significantly. In the state of the art energy harvesting wireless sensor SoC, a significant percentage of energy is lost in harvesting and supplying regulated output voltages for the sensor node, owing to the poor efficiency of harvester and voltage regulators. Also, wireless sensor nodes typically have a short burst of activity followed by a long idle time. This is done to save energy. The total power consumption of a sensor is often dictated by the power consumed in the idle mode. A clock source is often the only functional circuit in the idle mode which is used for time keeping for “wake up” and synchronization needs. For such SoCs, clock power determines the life-time.

This work focuses on the infrastructure circuits of a ULP SoC such as wireless sensors. It proposes highly efficient energy harvesters which can harvest solar and thermo-electric energy, efficient voltage regulators to provide power supplies for the SoC and ULP Clocking scheme to elongate the life time in idle mode. These circuits increase the amount of energy harvested from the ambient source, reduce the loss in voltage conversion and decrease the power consumption in idle mode.

1. Introduction

Ultra-Low Power (ULP) Systems on Chip (SoC) such as Body Sensor Nodes (BSNs) or Wireless Sensor Nodes (WSNs) promise to change the way we experience life by providing rich information about our activities, health, and the environment. These miniaturized nodes are responsible for sensing data periodically, processing it, and communicating information wirelessly. They can be used for hundreds of sensing applications – measuring and reporting everything from the flow of crude oil in a remote pipeline to the degree of corrosion in a steel bridge to EKG, EEG and EMG signals of a home health patient. Figure 1 shows the deployment of BSNs on a patient enabling his continuous health monitoring. These devices require small size and must consume extremely low power to be able to operate from harvested energy for their longer life time. Significant progress has been made over the last few years. Sensor nodes, which can operate from harvested energy without batteries, have been demonstrated [1]. However, there is a need to reduce the energy consumption of these nodes further for their extensive deployment in the environment. This is an ongoing research topic at various levels, from system to software to hardware. This thesis focuses on reducing the power consumption of a ULP SoC at the hardware level. It proposes improved energy harvesting and power management solutions, clock sources, a modeling framework to enable accurate power management, etc. These circuits and the model constitute the basic infrastructure for the efficient use of energy in a BSN.

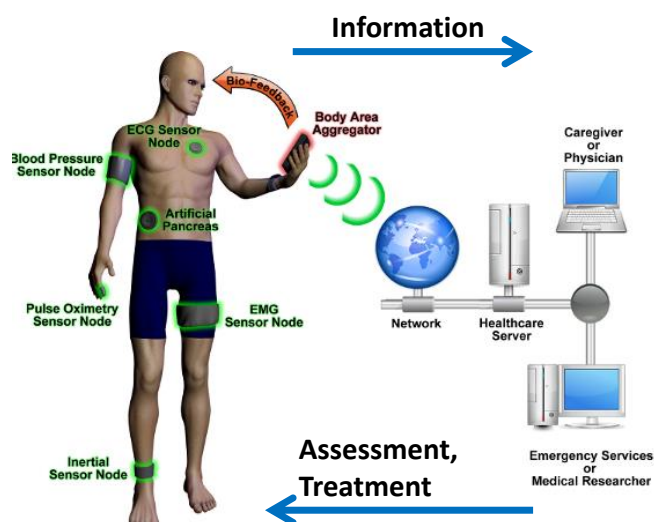


Figure 1. Deployment of Body Sensor Nodes

Figure 2 shows a BSN SoC which can operate from body heat. It has an Analog Front End (AFE) and Analog to Digital Converter (ADC) to perform sensing which can be ECG, EKG or other environmental sensing. The sensed data is sent for digital processing, which uses micro-controller, memory etc. The processed data is then transmitted through an RF transceiver to a nearby aggregator (For e.g. the Body Area Aggregator as shown in Figure 1). The SoC in Figure 2 harvests energy from a Thermo-Electric Generator (TEG) utilizing body heat. The energy harvester consists of a boost converter which collects the energy from the TEG at lower voltage and stores it at a higher voltage on a capacitor. Higher voltage is needed for proper operation of transistors in the SoC. Finally, voltage regulation block provides different power supply rails (VDDs) to run different blocks on the SoC such as analog, RF, etc.

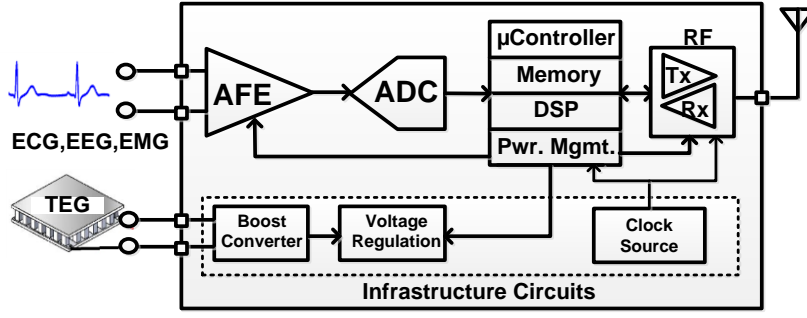


Figure 2. Energy Harvesting SoC [1]

A typical operation of a ULP SoC like BSN constitutes a short burst of activity followed by a long idle time. This is done to save energy. Figure 3 shows the power consumption profile of a BSN. The system wakes up first and starts the CPU. Analog blocks are then turned on to perform sensing application and finally, RF turns on for communication. The power consumption of the system rises in steps as each block turns on. The system goes back into sleep after completing the RF communication. These SoC use a real-time clock (RTC) for keeping time. RTC maintains precise timing for waking up and synchronization of the chip. Figure 3 also shows that the total power consumption of the chip can vary depending on application. For example, the power can be dominated by the active mode if the SoC has higher activity, and it will be dominated by the idle mode (RTC power) if the SoC has lower activity. There is a need to reduce and optimize the power consumption in both the regions of activity to elongate the system life time. This work proposes circuits which addresses both active and idle power consumption.

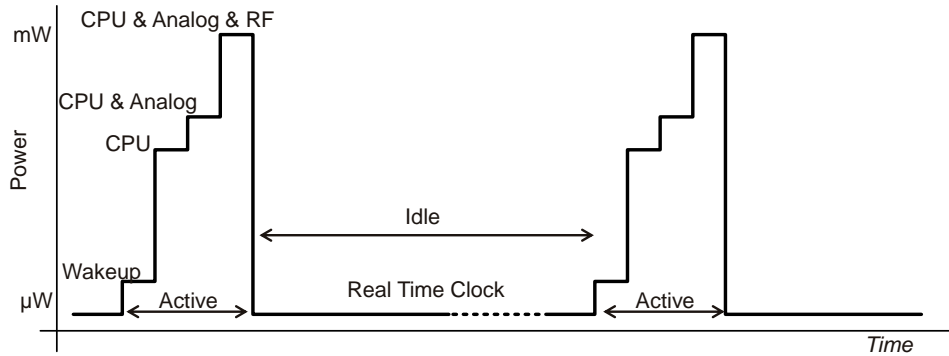


Figure 3. Typical Power Consumption Profile of a ULP SoC

The components of a SoC like AFE, RF, or CPU can change from system to system depending on the application. For example, the AFE needed for ECG can be quite different from the AFE needed to sense the flow of crude oil. However, each BSN SoC will need an energy harvester, voltage regulators and a clock source. These blocks constitute the basic infrastructure circuits needed for a ULP SoC like BSN. This dissertation focuses on these infrastructure circuits. It proposes alternative ULP circuits compared to the state of the art with lower power and lower cost solutions suited for BSN.

Figure 3 shows that the power consumption of a SoC, which stays in the idle mode for the majority of time, is dominated by the RTC. The RTC is typically implemented using an off-chip crystal resonator (XTAL). Their power consumption can be anywhere from few μW to hundreds of μW . This work presents ULP clock sources to reduce the power consumption in the RTC. A solution designed with an on-chip, silicon-based oscillator reduces the power consumption of the clock to 150nW. A locking scheme is proposed to lock the on-chip clock source to a known frequency. The proposed solution has been fabricated and demonstrated in silicon. A second version of the design brings the power down to 20nW. The proposed on-chip solution has a lower cost when compared to off-chip RTCs utilizing XTAL. Further, we also propose an alternate design of crystal oscillator reducing its power consumption to less than 1nW. This ULP XTAL can reduce the power consumption in RTC by few orders of magnitude. It can be used for applications where higher stability is preferred at the expense of cost. The proposed solution has been shown to work in simulation and is being fabricated for validation in silicon.

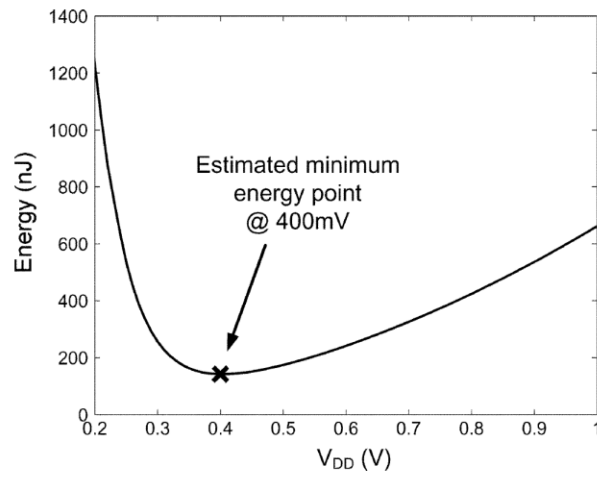


Figure 4 Optimal energy point of a block inside a SoC [2]

An optimal energy operating point exists for each block in a SoC [2]. Figure 4 shows the variation of energy consumption with V_{DD} . Various blocks of a BSN such as AFE, RF, or CPU need their own power supply voltage (V_{DD}) to be able to operate at optimal energy and performance point. Therefore, a BSN SoC needs multiple supply voltages apart from the energy harvesting interface. Conventional approaches to obtain and manage energy from ambient sources either employ more than one inductor, which increases the cost, or use low drop out (LDO) regulators which has lower efficiency. The lower efficiency of LDOs can result in the loss of energy which is not desirable. There is a need to provide an efficient and low-cost energy harvesting and power management solution for BSNs. This work proposes a highly efficient energy harvesting and power management solution with various design options for BSNs. The proposed solution can harvest energy from TEG and solar cells. It also proposes single inductor power management circuits with on-chip and off-chip decoupling capacitor options. The proposed solution saves up to 50% of energy on supply rails.

In addition, the thesis also presents a model which accurately establishes the benefits of power management techniques for ULP SoCs. The benefits of power management techniques like Dynamic Voltage and Frequency Scaling (DVFS) cannot be established accurately without assessing their impact

on the voltage regulators like DC-DC converter. For example, DVFS uses high voltage to support higher performance and lower voltage to save power. However, changing the output voltage of a DC-DC converter incorporates significant power overhead, and the efficiency can vary widely across voltage and current loads. These overheads may offset the benefits from DVFS. There is a need to measure the benefits of power management techniques like DVFS, clock gating, etc. in conjunction with their impact on the DC-DC converter. The proposed model enables the study of various power management techniques by taking into account their impact on DC-DC converters of different topologies.

The contributions of this dissertation will be:

- A stable on-chip clock source which can lock to a given clock frequency, a locking scheme to lock the clock source and ultra-low power on-chip clock sources
- A ULP crystal oscillator design
- A clock and data recovery (CDR) circuit for the RF interface of BSN
- A solar cell based single Inductor Energy harvesting and Power Management interface for the SoC.
- A peak inductor current control scheme for increasing the efficiency of voltage regulators.
- Single Inductor Multiple output Voltage regulators with on-chip decoupling capacitors
- A high efficiency (~90%), 50 mV input TEG based energy harvester and its maximum power point tracking scheme.
- A model which accurately establishes the benefits of power management techniques for ULP SoCs in the presence of voltage regulators

These contributions will help enable ULP SoCs like BSNs achieve its great promise for long term, comprehensive, inexpensive, and unobtrusive monitoring of patients and healthy individuals to run robustly on harvested energy.

The proposal is organized as follows. Chapters 2-4 cover the clock related portion of the proposal. Chapter 2 presents the on-chip clock source used for RTC while Chapter 3 presents the crystal oscillator. Chapter 4 presents a clock data recovery circuit for RF interface. Chapters 5 and 6 cover the energy harvesting and power management portion of the thesis. Chapter 5 covers the model which accurately establishes the benefits of power management techniques for ULP SoCs and Chapter 6 covers the energy management and harvesting circuits, which include voltage regulators, energy harvesters and related circuits.

2. Ultra Low Power Stable On-Chip Clock Source

2.1 Motivation

In an Integrated Circuit (IC) a clock source is used for various functions, which can include synchronous implementation of arithmetic and logic unit, inter-chip and intra-chip communication, time keeping, etc. The clock source constitutes a key component in an IC. It is extremely important for ULP SoCs like BSN. A typical BSN operation constitutes a short burst of activity followed by a long idle time. The total power consumption of a BSN is often dictated by the power consumed in the idle mode. A clock source is often the only functional circuit in the idle mode. It is used for time keeping for “wake up” and synchronization needs of the BSN. The clock source, therefore, can determine the power consumption of a BSN.

A clock source can be implemented either using off-chip components like a crystal resonator or using on-chip devices. An on-chip implementation of a clock source is lower in cost but poor in stability when compared to the off-chip implementation. In this chapter, we will present a stable on-chip clock source with stability close to its off-chip counterpart. The proposed circuit is suited for BSN and shows lower power and more stability compared to the state of the art. A corresponding off-chip solution for BSN using a crystal oscillator will be presented in chapter 3.

2.2 Introduction and Prior Art

BSNs typically require a stable clock source for precise data sampling, an RF modulation clock, and keeping time to reduce the cost of re-synchronizing to other radios. The conventional approach of using a crystal oscillator (XTAL) adds 3-4 off-chip passives, has startup times in the ms to second range, and can consume an appreciable fraction of the system power. For example, the energy harvesting BSN SoC in [1] consumes 19 μ W while measuring ECG, extracting heart-rate, and sending RF packets every few seconds, and over 2 μ W of that total is in the 200 kHz XTAL. The alternative clocking scheme to replace XTAL with low power and low cost on-chip reference oscillators for low power systems is an ongoing effort [3-6]. Widely varied approaches exist. In [6] authors present a CMOS relaxation oscillator. High temperature stability is achieved using poly and diffusion resistors together to realize the resistor in RC relaxation oscillator. These resistors have complementary temperature dependence, and they cancel the effect of temperature variation. It achieves temperature stability of 60ppm/ $^{\circ}$ C. On-chip oscillators using the gate leakage current has been proposed in [3-5]. Gate leakage current has small temperature dependence which makes these oscillators stable. However, these oscillators can operate only at extremely low frequency (0.1-10 Hz) owing to the low magnitude of gate-leakage current. Also, the oscillation frequency is not well controlled across process. The most stable oscillator [5] in this category has temperature stability of 32ppm/ $^{\circ}$ C operating at 0.4Hz. This work presents a new scheme to replace XTALs with an ULP on-chip clock source (no off-chip passives) for the \sim 100kHz range that is roughly 7X lower power and has temperature stability of 5ppm/ $^{\circ}$ C.

2.3 ULP On-Chip Clock Source

To maintain a stable on-chip clock source, we need a compensated oscillator (Osc_{CMP}). However, these circuits tend to consume power comparable to XTALs, in the few μ W range for \sim 100kHz. We propose a scheme to use an ULP uncompensated oscillator (Osc_{UCMP}) with the Osc_{CMP} to provide both stability and ULP consumption. Figure 5 shows the concept.

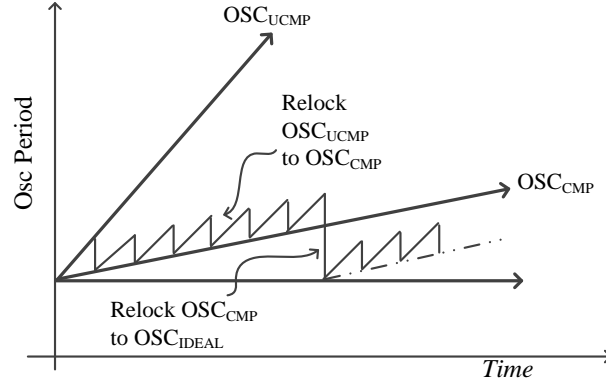


Figure 5. Scheme of Relocking low stability oscillator to achieve high effective stability

As temperature changes at a given rate, both oscillators will aggregate time error relative to the ideal reference, with OSC_{UCMP} accumulating error much faster due to its lower stability. If we periodically lock OSC_{UCMP} to OSC_{CMP} , then its effective stability stays within a bounded error of OSC_{CMP} , and we can make this error arbitrarily small by changing the duty cycle of re-locking. We can also re-lock to the original reference if it is available (e.g. XTAL or signal over RF). In between lock points, the higher power oscillator(s) can shut down, setting the system power to that of the OSC_{UCMP} . To make this work well, we need a fast locking circuit, low power oscillators with rapid turn on/off, and digital calibration storage. Figure 6 shows the architecture of the proposed clock source.

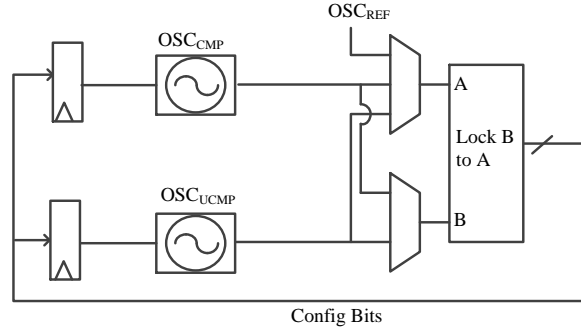


Figure 6. Architecture of Clock Source

2.4 Research Questions to be Addressed in Dissertation

- Can we achieve a highly stable on-chip clock source for BSN with ULP?
- How to lock one clock source to another?
- How often do we need to lock the low power clock source with stable clock in a BSN environment?
- What is the least power consuming on-chip OSC_{UCMP} for the given frequency of the clock source?
- How can we handle process variations for the clock source?

2.5 Research Questions that will not be Addressed in Dissertation

There are many important questions that are brought up by adapting the proposed on-chip clocking scheme. Since I cannot address them, I recommend the following for future work:

- Improvement in the locking scheme to address issue of jitter.
- Reduce the power supply dependency on Osc_{CMP} .
- A complete system around the clock source to execute various digital functionalities, like sending interrupts etc.

2.6 Hypothesis/Thesis

A scheme, which locks a low power uncompensated oscillator (Osc_{UCMP}) with a compensated oscillator (Osc_{CMP}) often, will result in a stable on-chip clock source with higher energy savings and a similar frequency stability when compared to the state of the art real-time clocks.

2.7 Approach

The proposed Osc_{CMP} uses a current starved ring oscillator that is designed to be stable across temperature, and that uses configuration bits to compensate for process variation. The oscillation frequency is set by current I_o and a capacitance C_L . To set the constant current I_o , we add the current from a weak inversion MOS (PTAT) and the current from a strong inversion MOS (CTAT). Current I_o varies by 1% over a $100^\circ C$ range ($100\text{ppm}/^\circ C$). We employ 2nd order compensation to further improve stability. We use configuration bits to compensate the effects of process variation on the constant current source and delay element. In the current source, variation may offset the PTAT and CTAT current so that one dominates in the target frequency range, making temperature stability impossible. We vary resistance R in the PTAT to balance its current with the CTAT against global variation using 5 bits. Similarly, we use 6-bit binary weighted off-transistors in the 2nd order compensation to align the leakage current to compensate for the process drift in leakage. We use the constant current source as an input to a binary weighted (8b) current mirror. This lets us generate the desired current for a given desired frequency across process. We include 10 bit coarse and 5 bit fine control for 1ns and 20ps resolution, respectively. This results in a Digitally Controlled Oscillator (DCO) that can lock to a desired frequency. The Osc_{UCMP} uses leakage (binary weighted off LV_T transistors) as the current source to the delay elements along with the same digital inverter based coarse and fine delay compensation as the Osc_{CMP} .

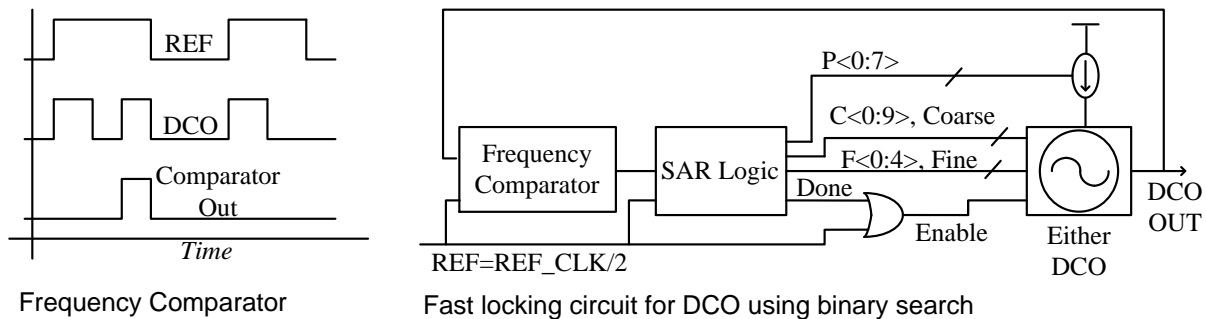


Figure 7. Locking Circuit for the Proposed Clocking Scheme

Figure 7 shows the locking scheme for clocks. We use a counter as a frequency comparator to compare Osc_{CMP} to a reference or Osc_{UCMP} to Osc_{CMP} . It counts rising edges of the DCO when the reference input is

high. If it counts more than 1, its output is high, else it is low. The proposed locking circuit comprises this comparator, SAR logic, and either DCO in a feedback configuration (Figure 7-b). The frequency comparator gives 1 when DCO's output frequency is higher than reference and 0 when it is lower. The SAR logic approximates the current and delay inside the DCO based on the output of the comparator and sets the 23 DCO control bits, which are stored in a register. The lock takes 46 reference cycles and has resolution error of ~ 20 ps.

We implemented the clock source in 130nm CMOS. Osc_{CMP} and Osc_{UCMP} consume $1\mu W$ and $100nW$ at 100kHz, 1.1V VDD, respectively. The process tuning bits give us a full measured locking range from 15kHz to 350kHz. In this range, we can lock successfully to the reference within the accuracy of jitter on the input clock. The measured stability of the Osc_{CMP} after calibration is at $5ppm/^{\circ}C$ in a BSN compatible range of $20-40^{\circ}C$ ($14ppm/^{\circ}C$ from $20^{\circ}C$ to $70^{\circ}C$). Without the 2nd order compensation, this stability degrades to $60ppm/^{\circ}C$. We lock Osc_{CMP} to a 100kHz reference, lock Osc_{UCMP} to Osc_{CMP} , then power down Osc_{CMP} . We can achieve high stability of $5ppm/^{\circ}C$ at ultra-low power of $150nW$.

2.8 Proposed Contributions

The proposed contributions are:

- A stable on-chip clock source for BSN with ULP.
- A fast locking circuit to lock one clock with another.
- An ultra-low power on-chip clock source consuming $100nW$. A further revision of the design brings this power down to $20nW$.
- Process compensation schemes.

2.9 Publications

A. Shrivastava, and B. H. Calhoun, "A $150nW$, $5ppm/^{\circ}C$, 100kHz On-Chip Clock Source for Ultra Low Power SoCs" *Custom Integrated Circuits Conference*. September 2012.

A. Shrivastava, and B. H. Calhoun. US Patent Application 61/698,534. "On-Chip Clock Source for Ultra Low Power SoCs"

3 A nW range 32.768Khz Crystal Oscillator for Real Time Clock in a BSN

3.1 Motivation

The total power consumption of a BSN is often dictated by the power consumed in the clock source. A silicon based oscillator providing an on-chip clock source was presented in Chapter 2. It provides a lower cost alternative clock source suited for BSN. The frequency stability of an on-chip oscillator, however, is not comparable to the off-chip oscillator using a crystal resonator (XTAL). The on-chip solution also needs calibration methods to compensate for manufacturing (process) and voltage variations in an IC. An XTAL uses mechanical resonance of piezoelectric material that provides extremely precise frequency. It is a frequency selective circuit whose output is independent of process or voltage variations. Conventional crystal oscillators consume few μW to hundreds of μW of power. It is not suitable for BSNs where the power consumption of the chip itself can be much lower (in nW). However, there is a need to provide high stability yet lower power clock source to make BSNs more robust. This chapter proposes an ultra-low power ($<1\text{nW}$) clock output at 32.768 kHz (which is used for real time clocks) in a BSN. This solution can be preferred over the on-chip solution presented in Chapter 2 if higher stability than on-chip clock is desired at the expense of cost.

3.2 Prior Art

A crystal is an electromechanical resonator which resonates at its natural frequency when excited with electrical energy. Figure 8 shows a conventional crystal oscillator circuit. The equivalent circuit of a crystal consists of a series RLC circuit with a parasitic parallel capacitor C_p . The frequency of oscillation is determined by L_m and C_m . The ESR represents the energy dissipating component of the crystal. The inverting amplifier, Amp provides the negative resistance which overcomes the loss from ESR and pumps energy into the crystal making it oscillate at its natural frequency.

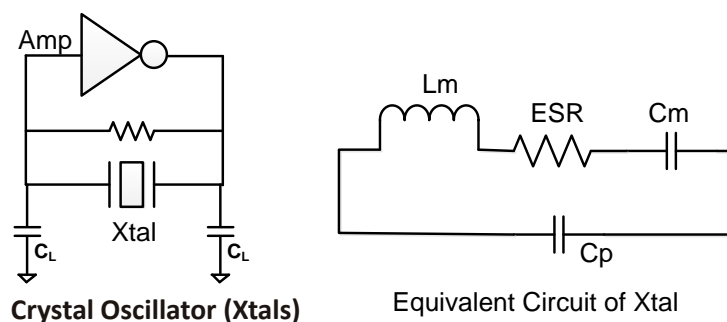


Figure 8 Crystal Oscillator Circuit

The energy dissipation of a crystal oscillator is determined by the voltage swing at the output of the oscillator and the amplifier. Higher swing results in a higher power dissipation as more energy is lost as heat in the ESR (I^2R loss). Lowering the swing voltage of crystal lowers power dissipation. However, at lower voltages Amp cannot provide required gain for the oscillation. The lowest reported power for a 32.768 kHz crystal using this scheme is 27nW [7]. A recent work reduces this power to 5.5nW [8] by using a delay locked loop (DLL) and two power supplies and two grounds. In this chapter, we present an

improved crystal oscillator with power less than 1nW utilizing single supply and ground. The proposed circuit also has lower area than prior work [8].

3.3 Research Questions to be Addressed in Dissertation

- What is the minimum VDD voltage at which crystal oscillator can be made to oscillate?
- Is it possible to switch the amplifier save the power and still be able to maintain the oscillation?
- How to establish the turn-on (TD) and turn-off (TG) time of amplifier correctly?
- Will the periodic switching of the amplifier result in frequency inaccuracy of the crystal oscillator?
- What is the least power consuming method for the level conversion of the crystal oscillator output to a higher digital voltage?

3.4 Research Question that will not be Addressed in Dissertation

There can be further improvement in the design, and I recommend the following for future work:

- What is the most efficient way to provide the VDD for the crystal oscillator consuming 1nW at 0.3V?
- How to address the temperature variation of TD and TG?

3.5 Hypothesis/Thesis

A 32.768 kHz crystal oscillator designed to operate in the sub-threshold region, where the amplifier of the oscillator can be periodically turned on and off, will consume lower energy and occupy lower area when compared to the state of the art crystal oscillators.

3.6 Approach

The power dissipated in crystal is dictated by the heat (I^2R) loss in its ESR and bias current in the amp. To reduce the power, oscillation swing has to be controlled. This can be achieved by operating the oscillator at the least possible V_{DD} [7]. In this work, we designed XTAL oscillator operating at 0.3V V_{DD} , being able to operate in sub-threshold voltage. To control the power dissipation, transistor of the amplifier are to be sized properly, increasing the size increases the negative resistance ($R_{Negative}$) but it also increases power. Decreasing the size makes $R_{Negative} < ESR$, failing to meet the oscillation criteria. To set the current properly in the amplifier for maintaining oscillation a 4 bit calibration circuit is proposed. It calibrates the size of the MOS transistors in the amplifier using an external resistor to set their sink current at 5-10nA. The length of the transistor is changed to source that current at 150mV ($V_{DD}/2$) using the SAR logic which sets the current correctly. This enables a 2-10nW XTAL oscillator. After the oscillation saturates effective $R_{Negative} = ESR$. The saturation of oscillation creates higher harmonics at XO resulting in unnecessary power dissipation. To save this power, the oscillation should not be allowed to saturate. We propose further improvements to save this power.

The energy of a crystal oscillator is stored in its inductor and capacitor. After the saturation of oscillation, if we remove the amp, the oscillation will start decaying, and if we connect it again it will start growing.

The power can be reduced further by switching the amp. The amplitude of oscillation is kept enough for the receiver to detect oscillation. Figure 9 shows the concept of the control scheme. When amp is disabled, the oscillation at XI will decay with a time constant (TD), which is determined by ESR and Lm. When amp is enabled, it grows with a time constant (TG), which is determined by R_{Negative} -ESR and Lm. For optimal power savings, the amp should be disabled for time proportional to TD, and enabled for time proportional to TG. A counter running on oscillator output frequency is enabled when the amplitude crosses set threshold. It counts till C1 and stops when amplitude crosses a higher threshold. This gives us digital o/p proportional to TG. Similarly, C2 proportional to TD can be obtained. A clock with the period (C1+C2) is obtained, with C1 as High and C2 as low as shown in Figure 9.

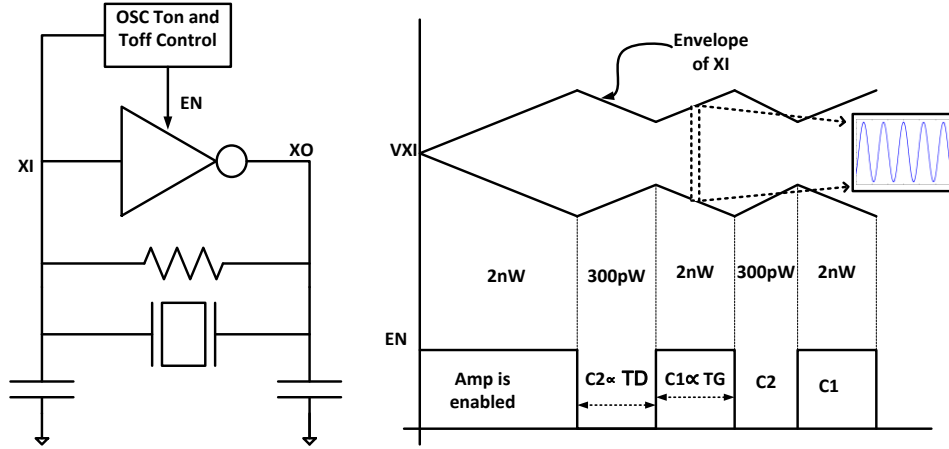


Figure 9. Proposed Control Scheme for XTAL to lower power consumption

The total power consumption of the crystal oscillator is given by the weighted average of on and off time power consumption. Since crystal oscillators have a high quality factor, both rise and decay of oscillation takes a lot of time. The growth of oscillation is roughly determined by the gain of the amp and decay by the ESR. By increasing the gain of the amp, the growth can be made faster, and its decay can take a long time. This way we obtain lower average amplitude of oscillation enabling a lower average power.

3.7 Proposed Contributions

The proposed contributions are:

- A sub-threshold crystal oscillator design.
- A mixed-signal scheme that obtains the TG and TD of a crystal oscillator
- A control scheme where amplifier can be disabled, yet oscillation can be retained utilizing the stored energy in the crystal resonator.
- A ULP level converter circuit for the conversion of crystal output at higher digital voltage

Publications

A. Shrivastava, et al, US Patent 8120439 “A Fast Start-up Crystal Oscillator”

4 Clock/Data Recovery Circuit in an RF Receiver on a BSN

4.1 Motivation

A BSN is responsible for sensing data periodically, processing it, and communicating information wirelessly. Since these devices require small size and long lifetimes, they must operate at very low power levels. The power needed for wireless communication can dominate a BSN's total power. RF transceivers used in BSNs undergo considerable performance degradation to meet power goals. Therefore, obtaining a fully-integrated low power end-to-end BSN SoC remains a challenge. The clock and data recovery (CDR) circuit is critical to achieving a low bit error rate (BER) for a BSN receiver. A CDR is used to recover data from the received signal in an RF communication. The recovered data is then used for digital processing. In this chapter, we present an ultra-low power CDR circuit that is used in our BSN SoC [1] that runs without a battery using harvested energy, which makes low power design essential.

4.2 Introduction and Prior Art

BSN uses RF transceiver for communication. Figure 10 shows the path of the received signal in a BSN chip. The RF signal is received in the presence of noise and other systematic variations. The received signal exhibits significant randomness that is termed as jitter. For example, the received signal in [9] has a jitter of $2\mu\text{s}$ for a data rate of 100kbps ($10\mu\text{s}$ period). The presence of jitter makes the data unintelligible for digital processing. Clock and data recovery (CDR) is needed to correctly recover the data. Figure 11 shows a conventional CDR circuit. It consists of a phase detector, loop filter and a voltage controlled oscillator (VCO), incorporating a phase locked loop (PLL) inside the CDR. The use of PLL is

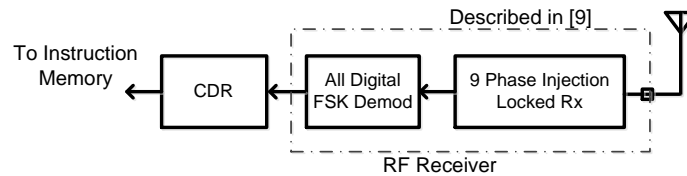


Figure 10. Receiver Data Path

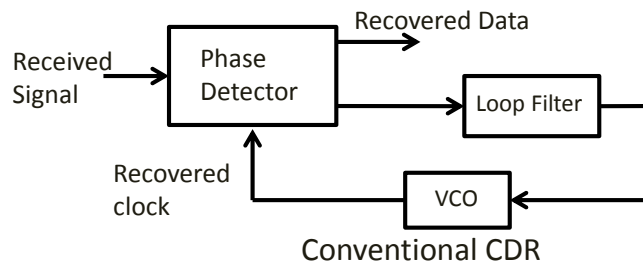


Figure 11. Conventional CDR Architecture

too costly in area and power for energy harvesting BSN applications. The design of a low power CDR for BSN is an ongoing effort [10-12]. In [10], 3b4b encoding of data is used to maximize the data transition and achieves a power of 217nW. [11] and [12] use PLL based CDR and have higher power consumption.

The BSN receiver [9] uses an all digital FSK demodulator to save power, and the proposed CDR captures the demodulator output.

4.3 Research Questions to be Addressed in Dissertation

- Is it possible to recover the data of an RF receiver without employing a PLL or a DLL?
- Can there be an all-digital implementation of CDR?
- What is the bit-error rate of the CDR?
- What is the power, area, and sensitivity tradeoff of the CDR?

4.4 Research Question that will not be Addressed in Dissertation

There can be several improvements in the design and I recommend the following for future work:

- Clock recovery is not adapted continually, which can lower the BER. A low power PLL based CDR can also be explored.

4.5 Hypothesis/Thesis

A clock and data recovery circuit, operating at sub-threshold voltage, enables the interface between RF receiver and digital processing in a BSN that consumes the least energy/bit of received data.

4.6 Approach

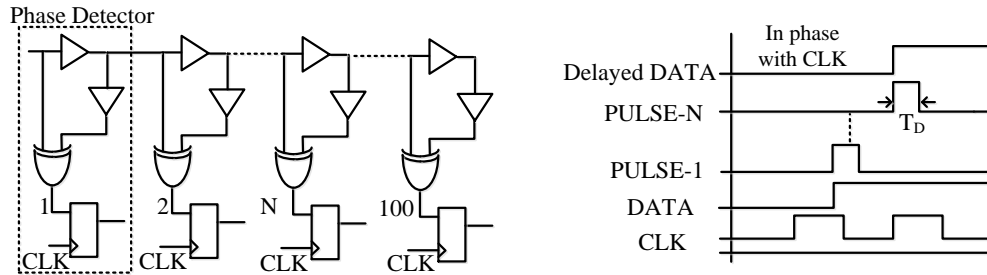


Figure 12. Phase Detection of Data

Figure 12 shows the phase detector (PD) circuit. A pulse generator at each delay point in the delay line generates a pulse of T_D when data makes a transition. This pulse feeds a D-Flip Flop (DFF) clocked by the oscillator at 200 kHz. If the pulse goes high around the point where clock goes high, the DFF catches the pulse, indicating that data is in-phase with the clock. A number of these phase detectors are placed in series. $T_D > 2 \cdot (T_{\text{Setup}} + T_{\text{Hold}})$ is a sufficient condition to ensure that at least one DFF goes high. We satisfy this condition for the most of the process points. One buffer delay sets the sensitivity of the delay line. Increasing the V_{DD} of CDR decreases delay through the buffer. This improves the sensitivity but increases the area and power as more stages are needed. $V_{DD} \sim 0.5V$ has 1% sensitivity, 1000X lower area, and 1000X lower power than at 1.2V. The SoC [1] digital V_{DD} is also 0.5V, so it was used for the CDR circuit. The point on the delay line where the DFF output goes high indicates the required delay in the data to bring it in phase with the clock. Monitoring these points over a few cycles can let us choose the correct point in the delay line to calibrate the sampling instant, much like a DLL.

However, it will increase the receiver energy to leave it on for a longer time. We choose to calibrate the circuit at the first calibration point in one-shot fashion. This minimizes the receiver on-time, which saves power. Once the delay point is selected, a control circuit is needed to output the data. Figure 13 shows the complete circuit diagram. The selected data is re-sampled at the falling edge of the clock. This removes the jitter in the data that will come in the subsequent cycles, up to half a clock cycle of jitter ($\sim 2.5\mu\text{s}$). The retention block keeps the net going into the DFF at ground before the calibration. Once the path is calibrated, the clock to the DFFs is gated using OROUT. The flops retain their values for the entire period of transmission. Once a transmission ends, the CDR resets. The proposed circuit is purely digital and hence can easily be synthesized.

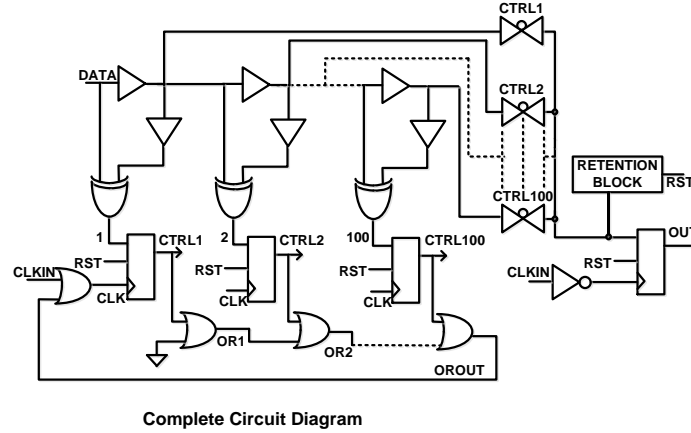


Figure 13 Complete Circuit Diagram of CDR Circuit

4.7 Proposed Contributions

The proposed contributions are:

- An easily synthesizable CDR circuit for BSNs.
- Design tradeoff between sensitivity, power, and area.
- Data recovery in the absence of a PLL or DLL
- Transmission gate based XOR gate has better performance in sub-threshold than standard cell XOR gate.

4.8 Publications

A. Shrivastava, and B. H. Calhoun, "A 50nW, 100kbps Clock/Data Recovery Circuit in an FSK RF Receiver on a Body Sensor Node" VLSI Design Conference. Jan. 2013.

Y. Zhang, F. Zhang, Y. Shakhshier, J. Silver, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19 uW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications", Journal of Solid State Circuit, Jan. 2013

F. Zhang, Y. Zhang, J. Silver, Y. Shakhshier, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", International Solid State Circuits Conference, Feb. 2012.

A. Shrivastava, and B. H. Calhoun, "A sub-threshold clock and data recovery circuit for a wireless sensor node", Sub-threshold Conference. Sept. 2011.

5 A DC-DC Converter Efficiency Model for System Level Analysis in Ultra Low Power Applications

5.1 Motivation

This chapter presents a model that accurately establishes the benefits of power management techniques for ultra low power (ULP) SoCs. Various power management techniques like dynamic voltage and frequency scaling (DVFS), clock gating, power gating, etc. are now commonly employed in many SoCs. However, the power benefits of these techniques cannot be established accurately without assessing their impact on the DC-DC converter that delivers power. For example, DVFS uses high voltage to support higher performance and lower voltage to save power. However, changing the output voltage of a DC-DC converter incorporates significant power overhead, and the efficiency can vary widely across voltage and current loads. These overheads may offset the benefits from DVFS. There is a need to measure the benefits of power management techniques like DVFS, clock gating, etc. in conjunction with their impact on the DC-DC converter. This is particularly important for ultra-low energy near- or sub-threshold systems that operate in a very dynamic power environment, and whose power constraints are stringent. This chapter presents a model that enables the study of various power management techniques by taking into account their impact on DC-DC converters of different topologies.

5.2 Prior Art

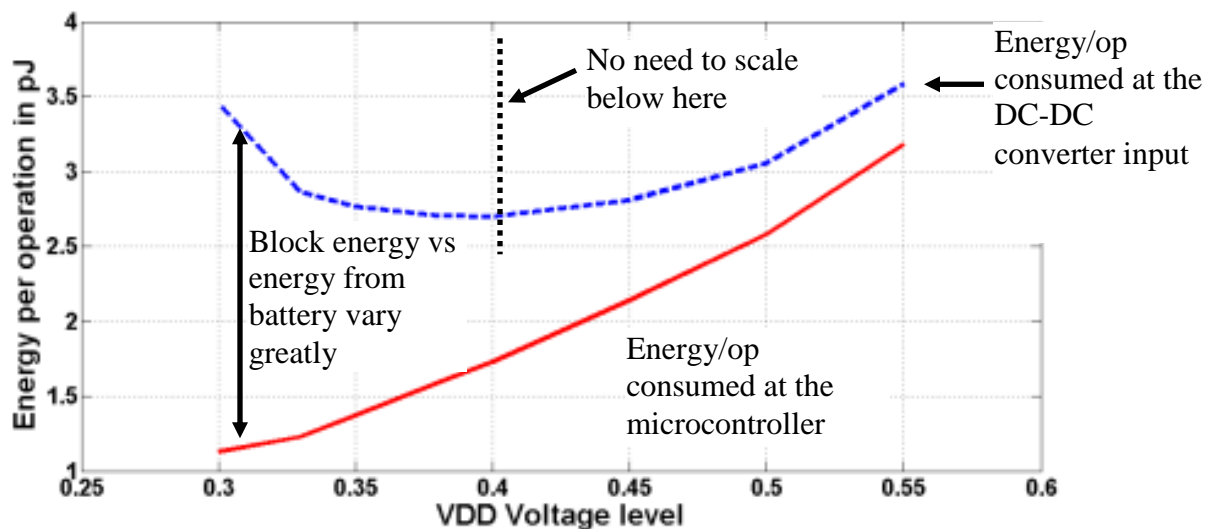


Figure 14 Energy Savings of DVFS with and without DC-DC overhead

The energy savings for a power management technique are typically reported at the operating voltage and load level in literature [13]. For example, the authors in [13] report the energy savings obtained by scaling the voltage and frequency to a lower value. It does not calculate energy from the source of the supply voltage, for example, a battery. Changing operating condition of a voltage regulator incurs deviation from its optimal behavior. If the output voltage of the converter is reduced, the efficiency of the converter degrades. Also, reducing the output voltage means that the decoupling capacitor C_L is discharged to a

lower voltage by dissipating its stored energy. The actual benefits can be obtained by taking these losses and overhead into account. Figure 14 shows the graphs of the energy savings measured at the microcontroller level and at the battery level. The graph at the battery level includes the DC-DC converter overhead using the proposed model. Figure 14 shows that DVS ceases to be beneficial after a given point. The proposed model accurately predicts the behavior of DC-DC converters across different operating points. It provides the change in the efficiency of the converter dynamically to accurately obtain the energy benefit or penalty in executing a power management technique by accounting for their dynamic voltage and load current changes.

5.3 Research Questions to be Addressed in Dissertation

- What role does DC-DC converter play in realizing the practical benefits of techniques like DVFS?
- What is the general trend of efficiency of a DC-DC converter with respect to supply voltage and load?
- Which scheme out of DVS and “panoptic” DVS better for energy savings?

5.4 Hypothesis/Thesis

A model of DC-DC converter, used to study power management techniques like DVFS, PDVS, etc., predicts the behavior of DC-DC converters of varying topologies across output voltage and current load and merits the relative strengths of different power management options.

5.5 Approach

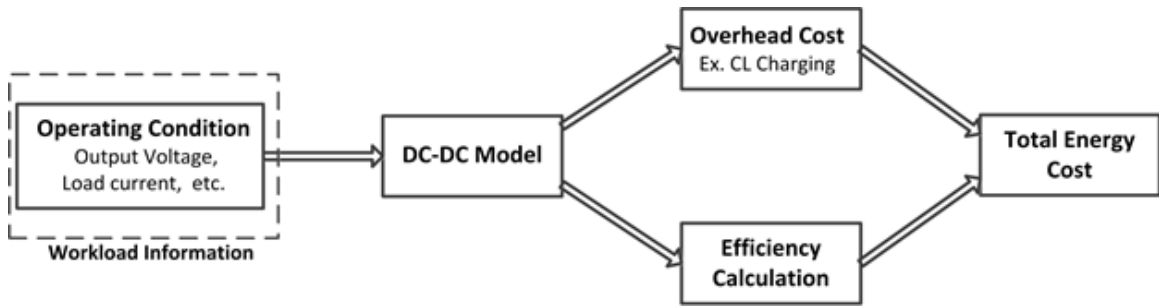


Figure 15 Structure of the proposed model

The proposed model of the DC-DC converter includes the current load information, voltage information, settling time, time of operation etc. to calculate the energy overhead. Figure 15 shows the usage of the proposed model to calculate the energy benefits of a given power management technique. It takes the operating condition of a workload as an input which includes the input voltage, V_i , output voltage, V_o , load current, I_L , time of operation TOP, etc. These parameters change dynamically in power management techniques like DVFS. Using these parameters as input, the model calculates the overhead cost and change in the efficiency of a DC-DC converter. Finally, it provides the actual energy consumed in executing a power management technique for the given workload profile. Figure 14 compares the power management benefits for the cases when DC-DC converter overhead is included and when it is not included.

5.6 Proposed Contributions

The proposed contributions are:

- Model of DC-DC converter across varying topology.
- Framework to obtain energy cost.
- Evaluation of various power management techniques in a dynamic work load environment.

5.7 Publications

A. Shrivastava, and B. H. Calhoun, "Modeling DC-DC Converter Efficiency and Power Management in Ultra Low Power Systems"" Sub-threshold Conference Oct-2012.

6 Energy Management and Harvesting Interfaces for Ultra Low Power Systems on Chip

6.1 Motivation

ULP SoCs like BSN can now operate from harvested energy obtained from ambient sources like solar cells or the body heat of a human being. It is vital that the energy is harvested efficiently and managed with minimum loss in order to enable battery less operation of BSNs. It is also vital that the energy harvesting and management circuit do not increase the cost or bill of materials (BOM) of the BSN which can hinder their wide spread deployment. Conventional approaches to obtain and manage energy from ambient sources either employ more than one inductor, which increases the cost and BOM, or use low drop out (LDO) regulators, which has lower efficiency. The lower efficiency of LDOs can result in the loss of energy which is not desirable. There is a need to provide an efficient and low cost energy harvesting and power management solution. This chapter proposes a highly efficient energy harvesting and power management solution with various design options. The proposed solution can harvest energy from TEG and solar cells. It also proposes single inductor power management circuits with on-chip and off-chip decoupling capacitor options.

6.2 Prior Art

Figure 16 shows the power management block of a BSN chip [1]. The BSN chip needs multiple rails for the optimal power performance. The existing power management solution for the chip includes multiple linear regulators and a switched capacitor regulator to supply different rails. A linear regulator such as an LDO suffers from poor efficiency. The theoretical maximum efficiency of an LDO cannot be more than V_{DD}/V_{BOOST} . Therefore, more than 63% 26% and 12% of energy on the V_{DD} rails, 0.5V, 1.0V, and 1.2V gets wasted in obtaining the regulated V_{DD} voltage. There is a need to provide energy efficient solutions for the power management which can increase the lifetime of the BSN chip. This work proposes a highly efficient energy harvesting and power management solution with various design options for BSNs. The proposed solution can harvest energy from TEG and solar cells. It also proposes single inductor power management circuits with on-chip and off-chip decoupling capacitor options. An on-chip version of SIMO is also proposed for PDVS scheme.

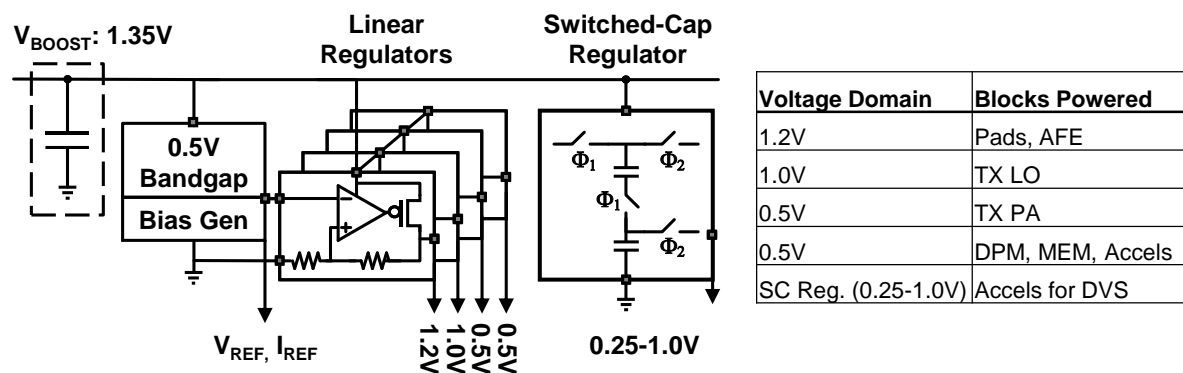


Figure 16 Top level diagram of supply regulation sub-system

6.3 Research Questions to be Addressed in Dissertation

- How to increase the energy efficiency of the voltage regulation circuit without increasing cost?
- What control scheme gives a high efficiency, yet lower quiescent current DC-DC converter?
- Is Single Inductor Multiple Output (SIMO) DC-DC converter a viable option for BSNs?
- Can PDVS supply voltages be implemented using on-chip capacitors
- How can we increase the efficiency of the boost converter energy harvester?
- How can we support battery interface on solar energy harvester?

6.4 Hypothesis/Thesis

A single inductor energy harvesting and power management interface circuit that harvests energy and supply multiple regulated voltages for a BSN SoC can provide energy and cost savings when compared to the prior art.

6.5 Approach

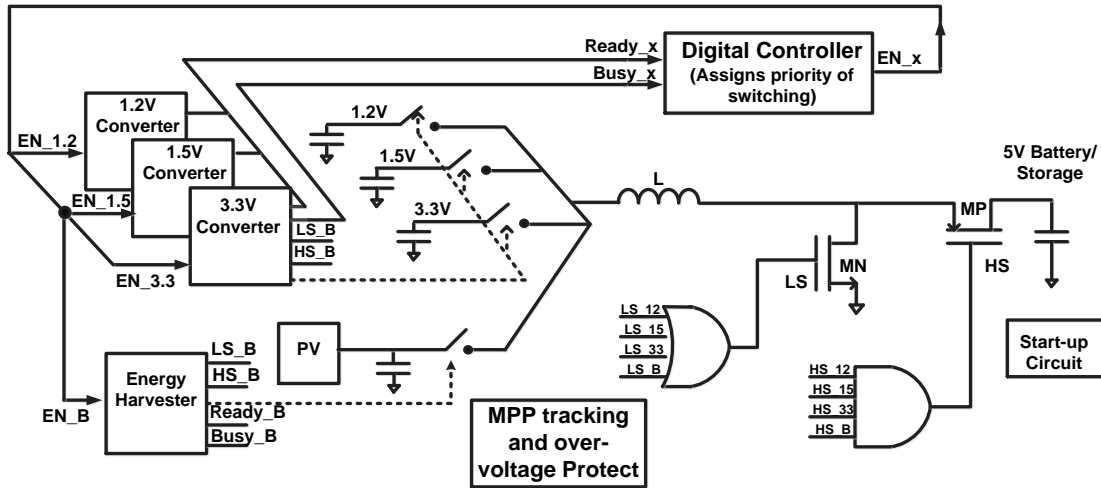


Figure 17. Proposed Energy Harvesting and Power Management Interface

We propose a low cost energy harvesting and power management circuits for Energy Harvesting SoCs like BSN [1]. The existing power management solution either uses LDOs [1] or uses more than one inductor [14]. Proposed solution uses Single inductor to efficiently harvest energy as well as provide multiple o/p voltages for SoCs at lower cost. It extends SIMO for BSNs. Figure 17 shows the architecture of one of the proposed energy harvester interface in the thesis. It includes three buck converters and one energy harvester for solar cell application. The inductor is shared by all the converters. Each converter is operated in Discontinuous Conduction Mode (DCM). The signals Busy and Ready indicate the state of inductor. Busy=H indicates that the given rail is getting charged, and Ready=H indicates that the given rail needs to be charged. Digital controller controls a converter by using Busy and Ready signals and assigns priority based on the load profile. A peak inductor current control scheme is proposed which

enables good efficiency for the regulated output voltages. The proposed scheme is less sensitive to mismatch and promises to be better than conventional current sensor scheme [15]. The proposed peak inductor current control scheme improves the efficiency and simplifies the architecture of the harvester. The switching control for each converter implements a pulse frequency modulation (PFM) scheme which scales the loss with load providing higher efficiency at light load conditions. The proposed circuit achieves close to 90% efficiency in simulations. A revision of this architecture implements energy harvester using a thermo-electric generator and achieves close to 90% efficiency at 50mV input voltage. We also implement a SIMO regulator with on-chip capacitors to implement PDVS power management scheme.

6.6 Proposed Contributions

The proposed contributions are:

- Single inductor energy harvesting and power management interface.
- A peak inductor current control scheme to increase the efficiency.
- A high voltage battery support for the energy harvester.
- A high efficiency energy harvester for TEG to utilize body heat.
- An offset compensating zero detection scheme.
- A SIMO with on-chip capacitors for PDVS.
- A hysteretic comparator control scheme for DC-DC converter with on-chip decoupling capacitor.

6.7 Publications

A. Shrivastava, Y. Ramadass, S. Bartling and B. H. Calhoun, “Single Inductor Energy Harvesting and Power Management Circuit for Body Sensor Nodes”, ISSCC SRP 2013

A. Shrivastava and Y. Ramadass, “Apparatus and Method for Controlling Peak Inductor Current in a Switched Mode Power Supply” US Patent application 13768448

A. Shrivastava, Y. Ramadass and S. Bartling, “Single Inductor Energy Harvesting and Management Interface System and Method” US Patent application

A. Shrivastava and B. H. Calhoun, “Single Inductor Multiple Output (SIMO) Step-down DC-DC Converter for Ultra Low Power SOCs” US Patent application 61/700979

7 Research Task

Table 1 below lists the tasks, status, and relevant publications for each research goal.

Table 1: Research task and status

Subject	#	Task Description	Status/Target	Publications
ULP-On Chip Clock Source	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	
	4	Test Chip	Done	[AS _p 4]
	5	Silicon Validation	Done	[AS5] [AS2][AS7][AS16]
ULP 32.768 kHz Crystal	1	Design Exploration	Done	[AS _p 5]
	2	Simulations	Done	
	3	Schematic/Layout	Done	
	4	Test Chip	Done	
	5	Silicon Validation	June 2013	[AS14][AS15][AS16]
CDR	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	[AS8]
	4	Test Chip	Done	
	5	Silicon Validation	Done	[AS1] [AS2][AS7]
DC- DC Model	1	Design Exploration	Done	
	2	Model generation	Done	
	3	Coding	Done	
	4	Model Validation	Done	[AS4][AS10]
Energy Harvesting and Power Management Interface	1	Design Exploration	Done	
	2	Simulations	Done	
	3	Schematic/Layout	Done	[AS3] [AS _p 1] [AS _p 2]
	4	Test Chip #1	Done	[AS _p 3]
	5	Test Chip #2	Done	
	6	Test Chip #3	Done	
	7	Silicon Validation #1	Done	[AS9]
	8	Silicon Validation #2	June 2013	[AS11][AS12]
	9	Silicon Validation #3	August 2013	[AS13]
Write up	1	Thesis Writing	Nov 2013	

8 Publications

6.1 Current Publications

- [AS1] A. Shrivastava, and B. H. Calhoun, "A 50nW, 100kbps Clock/Data Recovery Circuit in an FSK RF Receiver on a Body Sensor Node" VLSI Design Conference. Jan. 2013.
- [AS2] Y. Zhang, F. Zhang, Y. Shakhshere, J. Silver, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19 uW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications ", Journal of Solid State Circuit, Jan. 2013.
- [AS3] A. Shrivastava, Y. Ramadass, S. Bartling and B. H. Calhoun, "Single Inductor Energy Harvesting and Power Management Circuit for Body Sensor Nodes", ISSCC SRP 2013.
- [AS4] A. Shrivastava, and B. H. Calhoun, "Modeling DC-DC Converter Efficiency and Power Management in Ultra Low Power Systems"" Sub-threshold Conference Oct-2012.
- [AS5] A. Shrivastava, and B. H. Calhoun, "A 150nW, 5ppm/o C, 100kHz On-Chip Clock Source for Ultra Low Power SoCs" Custom Integrated Circuits Conference. Sept. 2012.
- [AS6] A. Shrivastava, J. Lach, and B. H. Calhoun, "A Charge Pump Based Receiver Circuit for a Voltage Scaled Interconnect" International Symposium on Low Power Electronics and Design, Jul. 2012
- [AS7] F. Zhang, Y. Zhang, J. Silver, Y. Shakhshere, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", International Solid State Circuits Conference, Feb. 2012.
- [AS8] A. Shrivastava, and B. H. Calhoun, "A sub-threshold clock and data recovery circuit for a wireless sensor node", Sub-threshold Conference. Sept. 2011.

6.2 Anticipated Publications

- [AS9] SIMO for PDVS paper submitted to VLSI
- [AS10] DC-DC Model, journal article submitted to JLPEA
- [AS11] Energy Management and Harvesting, [conference paper]
- [AS12] Energy Management and Harvesting, [Journal]
- [AS13] TEG based boost converter
- [AS14] ULP XTAL oscillator
- [AS15] BSN chip rev-2
- [AS16] Clock chip system

9 Patents

6.3 Issued or Pending Patents

[AS_p1] A. Shrivastava, and Y. Ramadass, “Apparatus and Method for Controlling Peak Inductor Current in a Switched Mode Power Supply” US Patent application 13768448

[AS_p2] A. Shrivastava, Y. Ramadass, and S. Bartling, “Single Inductor Energy Harvesting and Management Interface System and Method” US Patent application

[AS_p3] A. Shrivastava, and B. H Calhoun, “Single Inductor Multiple Output (SIMO) Step-down DC-DC Converter for Ultra Low Power SOCs” US Patent application 61/700979

[AS_p4] A. Shrivastava, and B. H. Calhoun. US Patent Application 61/698,534. “On-Chip Clock Source for Ultra Low Power SoCs”

[AS_p5] A. Shrivastava, et al, US Patent 8120439 “A Fast Start-up Crystal Oscillator”

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- [11] S-J Song, N. Cho, and H-J Yoo, "A 0.2-mW 2-Mb/s Digital Transceiver Based on Wideband Signaling for Human Body Communications", *IEEE Journal on Solid State Circuit*, Sept. 2007
- [12] S. Kim, et. al, "A low-power referenceless clock and data recovery circuit with clock-edge modulation for biomedical sensor applications", *IEEE International Symposium on Low Power Electronics and Design*, Aug. 2007
- [13] S. M. Martin, K. Flautner, T. Mudge and D. Blaauw, "Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads," *International Conference on Computer Aided Design* 2002.
- [14] K. Kadrivel, et al, "A 330nA energy-harvesting charger with battery management for solar and thermoelectric energy harvesting" *IEEE International Solid State Circuits Conference*, Feb. 2012
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